#39/Appeal Brief
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Pan et al.

Serial No.: 09/259,145

Filed: February 25, 1999

For: WELL-DRIVE ANNEAL TECHNIQUE USING PREPLACEMENT OF NITRIDE FILMS FOR ENHANCED FIELD ISOLATION

Examiner: Anh D. Mai

Group Art Unit: 2814

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APPEAL BRIEF

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in TRIPLICATE pursuant to 37 C.F.R.§ 1.192(a) and in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c):

(1) REAL PARTY IN INTEREST

The real party in interest to the referenced application is Micron Technology, Inc., a corporation of the State of Delaware, having a place of business at 8000 South Federal Way, Boise, Idaho 83707-0006, the assignee of the entire right, title and interest for the referenced application in the United States and all foreign countries.

(2) RELATED APPEALS AND INTERFERENCES

The Appellants, the Appellants' representative, and the assignee are not aware of any pending appeal or interference that would directly affect, be directly affected by, or have some bearing on the Board's decision in the present pending appeal.

(3) STATUS OF CLAIMS

Claims 25, 26, 31-34, 37-40, and 43-49 are currently pending in the above-referenced patent application. Claims 25, 26, 31-34, 37-40, and 43-49 stand rejected. The rejections of claims 25, 26, 31-34, 37-40, and 43-49 are being appealed.

(4) STATUS OF AMENDMENTS

The last amendment to the claims of the referenced patent application entered by the United States Patent and Trademark Office was submitted in an Amendment filed on May 28, 2002.

Claims 25, 26, 31-34, 37-40, and 43-49 were subsequently rejected in the Final Office Action dated July 29, 2002.

On September 10, 2002, Appellant filed a Response under 37 C.F.R. § 1.116, in which no amendments were made to the pending claims.

In an Advisory Action dated September 30, 2002, the rejections of claims 25, 26, 31-34, 37-40, and 43-49 were maintained.

A Notice of Appeal in the referenced application was mailed on October 21, 2002.

(5) SUMMARY OF THE INVENTION

Among other things, the referenced application discloses an intermediate structure in the formation of an isolation structure for a semiconductor device. With reference to FIGs. 1-8 of the referenced application, clean, informal copies of which are included as Appendix B for the sake of convenience, an exemplary embodiment of the intermediate structure disclosed in the referenced application includes a substrate 102 that has a first surface 104 and a second surface 106 that opposes the first surface 104. The substrate 102 also includes p-wells 108 and n-wells 110, into which n-type areas 114 and p-type areas 116 are implanted. A pad oxide film 118 is grown on the first surface 104 of the substrate 102.

A diffusion barrier layer 120 is deposited over the pad oxide film 118 to produce an encapsulated structure 121. The diffusion barrier layer 120 is formed from silicon nitride or silicon oxynitride. The encapsulated structure 121 is annealed in an ambient atmosphere of inert gas to activate the n-type areas 114 and the p-type areas 116. After annealing, a photo mask

material 122 is applied over the diffusion barrier layer 120 and a dry etch process is used to define active device areas 124. After the mask material 122 is stripped, a field oxide 130 is grown on the first surface 104. Portions of the field oxide 130 are removed and the diffusion barrier layer 120 is removed to form field isolation structure 132.

Since the n-type and p-type areas are formed and activated before the field isolation structures 132 are formed, the encroachment of the field isolation structures 132 into the active device areas 124 is reduced. In addition, since the substrate 102 is encapsulated before the n-type and p-type areas are activated (annealed), metal contamination of the substrate 102 is reduced.

(6) ISSUES

(A) Whether claims 25, 26, 31, 33, 34, 37-40, and 43-48 are patentable under 35 U.S.C. §103(a) over United States Patent No. 5,545,577 to Tada ("Tada") in view of United States Patent No. 5,874,325 to Koike ("Koike"); and

(B) Whether claims 32 and 49 are patentable under 35 U.S.C. § 103(a) over Tada and Koike and further in view of United States Patent No. 5,846,596 to Shim *et al.* ("Shim").

(7) GROUPING OF CLAIMS

Group 1: Claims 25, 26, 31-34, 37, 38, and 46-49:

Claims 25, 26, 31-34, 37, 38, and 46-49 are grouped together. Appellants respectfully submit claim 33 is the broadest claim of the group. Claims 25, 26, 31-34, 37, 38, and 46-49 stand together. Claims 32 and 49 stand but do not fall with claims 25 and 46.

Group 2: Claims 39, 40, 43, 44, and 45:

Claims 39, 40, and 43-45 are grouped together. Claims 40, and 43-45 stand and fall with claim 39.

(8) ARGUMENT

(A) Rejection under 35 U.S.C. § 103(a)-Tada and Koike

(1) Arguments for the Patentability of Claims 25, 26, 31, 33, 34, 37-40, and 43-48

Claims 25, 26, 31, 33, 34, 37-40, and 43-48 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tada in view of Koike. Appellants respectfully traverse these rejections as detailed herein.

To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art, and not be based on Appellants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

In establishing a motivation to combine, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01; see *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). To support a *prima facie* case of obviousness, there must be an objective reason to combine the teachings of the references when the references relied upon teach that all aspects of the claimed invention are individually known in the art. M.P.E.P. § 2143.01; see *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993).

Tada discloses "a semiconductor device capable of obtaining a high withstand voltage property." Column 2, lines 59-60. In forming the semiconductor device, a first gate insulating film is formed without being contaminated by a resist layer. Column 2, lines 58-67. As a result, gate oxides of different thicknesses are produced without contacting the resist layer. Specifically, a silicon substrate having impurities in p and n channel type metal oxide semiconductor field effect transistor ("MOSFET") formation regions is prepared. The impurities are diffused to form an n well and a p well, during which a base oxide film is formed on the surface of the silicon substrate. Column 6, lines 3-19. A p-type offset diffusion layer is formed in the p channel type MOSFET formation region and an n-type offset diffusion layer is formed in the n channel type MOSFET formation region. FIG. 2c; column 6, lines 20-26. n^+ and p^+ type guard rings are formed to isolate the MOSFET. FIG. 3a; column 6, lines 26-29. Subsequently, a silicon nitride mask is used to form a field oxide film. Column 6, lines 27-31. The base oxide film is then removed and a wet oxidation is performed to form a thick gate oxide film. Column 6, lines 32-37. The base oxide film in Tada is not a barrier layer and is not dopant-free because it is formed

on the semiconductor substrate before the diffusion layers are formed. In addition, the diffusion layers are interrupted layers that do not extend over either a first surface or a second surface of the semiconductor substrate.

Koike discloses a method of manufacturing a semiconductor device that includes forming a gettering layer, which is a silicon thin film to which impurities have been added, on a reverse surface of a silicon substrate. Column 3, lines 56-64; Column 6, lines 56-60. The gettering layer "prevents the deterioration of electrical characteristics of the device" caused by contamination with metal impurities. Column 1, lines 5-10. The silicon thin film (gettering layer) and a silicon nitride film are applied to both surfaces (an obverse surface side and a reverse surface side) of the semiconductor surface. Column 6, line 65-column 7, line 2. A resist is applied over the silicon nitride film and is patterned to form a resist pattern that is used to form an element separation region. Column 6, lines 61-65. The silicon nitride film is etched, using the silicon thin film as an etch stop, and the resist pattern is removed. Column 7, lines 7-10. The silicon thin film and the silicon nitride film are subsequently removed from the obverse surface side and a gate oxide film, a gate electrode, and source and drain diffusion layers are formed to produce a MOSFET on the semiconductor substrate. Column 7, lines 16-23. The silicon nitride film on the reverse surface side remains in place to act as a "cover and assist in rendering the silicon thin film" as a gettering layer until the manufacturing process is complete. Column 7, lines 24-32. Therefore, the silicon nitride film on the obverse surface side is substantially compromised during the formation of field oxide regions and is removed before doped areas are formed on the semiconductor substrate.

(a) Claims 25, 26, 31, 33, 34, 37, 38, and 46-49

Independent claim 25 recites an intermediate structure in the formation of an isolation structure that, among other things, includes a semiconductor substrate having at least a portion that is free of field oxide structures. The semiconductor substrate also has a first and a second opposing surface. The semiconductor substrate has at least one p-well and at least one n-well on its first surface. The at least one p-well comprises at least one activated, annealed n-type area and the at least one n-well comprises at least one activated, annealed p-type area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion layer that extends over both the first and second surfaces of the substrate to encapsulate the semiconductor substrate.

Independent claim 33 recites an intermediate structure in the formation of an isolation structure for a semiconductor device. The intermediate structure comprises a semiconductor substrate having at least a portion free of field oxide structures and having a first surface opposing a second surface. The substrate first surface includes at least one p-well and at least one n-well. At least one activated, annealed doped area is located within at least one of the n-wells and the p-wells. A substantially dopant-free, uninterrupted diffusion barrier layer extends over the first surface and the second surface of the semiconductor substrate to encapsulate the semiconductor substrate.

Independent claim 46 recites an intermediate structure useful in the formation of electrical device isolation structures. The intermediate structure comprises a semiconductor

substrate that has at least a portion that is free of field oxide structures. The semiconductor substrate also includes a first surface and a second surface, with the first surface opposing the second surface. The semiconductor also has at least one p-well and at least one n-well defined on the first surface. In addition, at least one activated, annealed p-type area is defined within the at least one n-well and at least one activated, annealed n-type area is defined within the at least one p-well. A substantially dopant-free, uninterrupted diffusion barrier layer extends over the first and second surfaces to encapsulate the semiconductor substrate.

A *prima facie* case of obviousness of claims 25, 33, and 46 has not been established because Tada and Koike do not motivate one of ordinary skill in the art to combine the teachings of the cited reference to produce the claimed invention.

(i) There Is No Motivation to Combine the Cited References to Produce the Invention of Independent Claims 25, 33, and 46

It is respectfully submitted that one of ordinary skill in the art would not be motivated to combine the teachings of Tada and Koike to produce the invention of claims 25, 33 and 46 because neither of the cited references suggests the desirability of , nor provides an objective reason for, the combination.

As acknowledged by the examiner, Tada does not teach or suggest a substantially dopant-free, uninterrupted diffusion barrier layer that extends over the second surface of the substrate. Office Action of July 29, 2002, page 3. Therefore, Tada does not disclose that the semiconductor substrate is encapsulated. Appellants respectfully submit that Tada also does not teach or suggest

a substantially dopant-free, uninterrupted diffusion barrier layer that extends over the first surface of the substrate. The Examiner asserts that Tada teaches this limitation and cites to column 6, lines 3-32, FIG. 2C, and FIG. 3A of Tada, which describes diffusion layers 5 and 6 and base oxide film 4. Office Action of July 29, 2002, page 3. While it is unclear which of these three structures the Examiner is referring to, Appellants submit that none of these structures are a substantially dopant-free, uninterrupted diffusion barrier layer that extends over the first surface of the substrate. The diffusion layers 5 and 6 are not substantially dopant-free, uninterrupted diffusion barrier layers because they are interrupted layers and, as such, do not extend over the first surface of the semiconductor substrate. Base oxide film 4 also is not the substantially dopant-free, uninterrupted diffusion barrier layer because it is not a diffusion barrier layer. Furthermore, base oxide film 4 is not substantially dopant-free because it is formed on the semiconductor substrate before diffusion layers 5 and 6 are formed. Since Tada does not teach or suggest a substantially dopant-free, uninterrupted diffusion barrier layer that extends over the first or the second surfaces of the semiconductor substrate, Tada does not provide the desirability of encapsulating the semiconductor substrate.

Assuming *arguendo* that Tada does teach or suggest all the limitations of the rejected claims, the cited references, in combination, nevertheless do not provide a suggestion or motivation to combine to produce the claimed invention because neither suggests the desirability of, nor provides an objective reason for, the combination.

Tada does not suggest the desirability of, or provide an objective reason for, combining the cited references to produce an intermediate structure having a substantially dopant-free,

uninterrupted diffusion barrier layer that extends over the first and second surfaces of the semiconductor substrate. Nothing in Tada contemplates encapsulating the semiconductor substrate, let alone encapsulating the semiconductor substrate with a substantially, dopant-free uninterrupted diffusion barrier layer. Since Tada does not teach the desirability of a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first surface or the second surface of the substrate, for the reasons previously discussed, Tada does not contemplate such a diffusion barrier layer extending over both the first and second surfaces of the substrate. Thus, one of ordinary skill in the art would not be motivated, after reading Tada and Koike, to form an intermediate structure having a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate, as recited in claims 25, 33, and 46.

While Koike discloses that its silicon nitride film extends over the first and second surfaces of its substrate to render gettering properties to the underlying silicon thin film, Koike does not suggest the desirability of, or provide an objective reason for, forming a silicon nitride layer on both surfaces of other semiconductor substrates. Therefore, one of ordinary skill in the art would not be motivated after reading Koike and Tada to form an intermediate structure that has a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate, as recited in claims 25, 33, and 46.

In addition, Koike teaches away from the combination with Tada because in Koike, the activated, annealed areas are not present while the silicon nitride films encapsulate the substrate. Rather, the silicon nitride film on the obverse surface side of the substrate is patterned during the

formation of the field oxide regions and is removed before the doped areas are formed on the semiconductor substrate. Column 7, lines 11-23; FIGs. 13 and 14. Therefore, the structure in Koike does not have activated, annealed areas while the substrate is encapsulated by the silicon nitride films.

The Examiner states that it would have been obvious to one of ordinary skill in the art to encapsulate the semiconductor substrate of Tada to prevent the second surface from oxidizing. Office Action of July 29, 2002, page 3. While the nature of the problem to be solved is a potential source of a motivation to combine, the cited references and the claimed invention in the present case do not address the same, or even similar, problems. M.P.E.P. § 2143.01. Furthermore, the cited references and the claimed invention do not address the problem identified by the Examiner. Nothing in Tada or Koike teaches or suggests preventing oxidation of the surface of the semiconductor substrate or suggests that encapsulating the semiconductor substrate would solve this problem. The substrate in Tada is not encapsulated while the substrate in Koike is encapsulated to protect the gettering properties of the underlying silicon thin film layer until the manufacturing process is complete. Therefore, one of ordinary skill in the art would not be motivated to combine the cited references to produce the claimed invention to prevent oxidation on the surface of the semiconductor substrate, as asserted by the Examiner.

The claimed invention also does not disclose that its semiconductor substrate is encapsulated to prevent oxidation of the surface. Rather than preventing oxidation, the claimed invention reduces the encroachment of field oxide structures. Nothing in Tada and Koike teaches or suggests reducing encroachment of field isolation structures and, therefore, one of ordinary

skill in the art would not have been motivated to combine the cited references to produce the claimed invention.

Appellants also respectfully submit that the Examiner's proposed motivation to combine is not an objective reason to combine the cited references that is based on properly supported findings. As explained by the United States Court of Appeals for the Federal Circuit, "it is fundamental that rejections under 35 U.S.C. § 103 must be based on evidence." *In re Lee*, 61 U.S.P.Q.2d 1430, 277 F.3d 1338, 1342 (Fed.Cir. 2002). This evidence "must be based on objective evidence of record." *Id.* at 1343. When patentability depends on a question of obviousness, "rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references" is "the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis." *Id.* This rigorous showing requires the Examiner to "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." *Id.* In other words, the motivation to combine can not "be resolved on subjective belief and unknown authority." *Id.* at 1344. Furthermore, the Examiner "cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies." *Id.* at 1345.

The Examiner's statement that it would be obvious to encapsulate the semiconductor substrate of Tada to prevent the second surface from oxidizing is conclusory and is not based on any findings or rationale. The Examiner has not presented any objective evidence that one of ordinary skill in the art would have been motivated to combine the cited references to produce

the claimed invention. On the contrary, in every office action detailing this rejection, the Examiner has stated, conclusorily, that the combination would have been obvious to prevent the second surface from oxidizing.

The Examiner also asserts that Appellants have "silently" agreed to the motivation to combine. Office Action of July 29, 2002, page 6. However, Appellants have never agreed to a motivation to combine and have repeatedly argued against any such motivation to combine. The Examiner identified one response where Appellants did not argue against the motivation to combine and instead argued that the claimed invention was not obvious because the cited references did not teach or suggest all the claim limitations. By doing so, Appellants did not acquiesce to the motivation presented by the Examiner or waive their right to further argue this issue. Appellants are not required to present every reason or argument for patentability in each and every response to the office action during the course of the prosecution of a case. To require this would ensure that responses to office actions would be extraordinarily lengthy.

Appellants have not acquiesced to the motivation to combine because in at least eight responses, Appellants have argued against any motivation to combine. See for example Appellants' response filed on May 28, 2002; Appellants' response filed on October 15, 2001; Appellants' supplemental response to final rejection filed on July 5, 2001; Appellants' response filed on April 12, 2001; Appellants' response filed on November 28, 2000; Appellants' response filed on July 14, 2002; Appellants' response filed on June 19, 2000; and Appellants' response filed on February 3, 2000. These responses have consistently argued against the Examiner's

proposed motivation to combine and indicate that Appellants strongly contest that a motivation to combine the cited references exists.

The Examiner also states that the Appellants' arguments on obviousness are directed to the individual references. However, Appellants' arguments are directed to the combination of the cited references. Specifically, Appellants' arguments point out that there is no motivation or suggestion to combine the cited references to produce the claimed invention.

It is submitted that since Tada and Koide do not suggest the desirability of, or provide an objective reason for, the proposed combination, the cited references do not provide one of ordinary skill in the art with any motivation to combine their teachings. Rather, any such motivation to combine must be impermissibly based on hindsight provided by the disclosure of the referenced application, from which certain teachings were gleaned and picked from Tada and Koike.

Since Tada and Koike do not provide a motivation to combine the cited references, it is respectfully submitted that a *prima facie* case of obviousness of independent claims 25, 33, and 46 has not been established. Accordingly, under 35 U.S.C. § 103(a), claims 25, 33, and 46 are allowable over Tada and Koike.

Claims 26 and 31 are each allowable, among other reasons, as depending directly from allowable claim 25. A dependent claim is obvious only if the independent claim from which it depends is obvious. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); M.P.E.P. § 2143.03. Claims 26 and 31 depend from claim 25 and, therefore, include all the limitations of allowable

claim 25. Since Tada and Koike do not establish a *prima facie* case of the obviousness of claim 25, the nonobviousness of independent claim 25 precludes the rejections of claims 26 and 31.

Claims 34, 37, and 38 are each allowable, as depending directly from allowable claim 33. Since claims 34, 37, and 38 depend from claim 33, they include all the limitations of claim 33. The nonobviousness of independent claim 33 precludes the rejections of claims 34, 37, and 38 because, as previously discussed, Tada and Koike do not establish a *prima facie* case of the obviousness of claim 33.

Claims 47 and 48 are each allowable, among other reasons, as depending directly from allowable claim 46. Claims 47 and 48 depend from claim 46 and, therefore, include all the limitations of claim 46. The nonobviousness of independent claim 46 precludes the rejections of claims 47 and 48 because, as previously discussed, Tada and Koike do not establish a *prima facie* case of the obviousness of claim 46.

(b) Claims 39, 40, 43, 44, 45

Claim 39 recites an intermediate structure in the formation of an isolation structure for a semiconductor device. The intermediate structure comprises a semiconductor substrate that has at least a portion free of field oxide structures. The semiconductor substrate also has a first surface that opposes a second surface. The semiconductor substrate has at least one activated, annealed first doped area on its first surface and at least one activated, annealed second, differently doped area within the at least one first doped area. The intermediate structure also comprises a substantially dopant-free, uninterrupted diffusion barrier layer that extends over the

first and second surfaces of the semiconductor substrate to encapsulate the semiconductor substrate.

A *prima facie* case of obviousness of claim 39 has not been established because one of ordinary skill in the art would not have been motivated to combine the teachings of Tada and Koike to produce the claimed invention.

(i) The Cited References Do Not Provide a Motivation to Combine

Claim 39 is allowable over Tada and Koike because the cited references do not provide a motivation to combine. Specifically, the cited references do not suggest the desirability of, or provide an objective reason for, the combination. Tada does not teach or suggest a substantially dopant-free, uninterrupted barrier layer that extends over the first surface of the substrate because its layers on the first surface are interrupted. Since Tada does not teach or suggest the uninterrupted diffusion barrier layer, Tada necessarily does not teach or suggest that the semiconductor substrate is encapsulated by an uninterrupted diffusion barrier layer that extends over the first and second surfaces. Tada also does not teach or suggest that the semiconductor substrate has at least one activated, annealed first doped area on its first surface and at least one activated, annealed second, differently doped area within the first doped area. Thus, Tada does not suggest the desirability of, or provide an objective reason for, combining the cited references.

While Koike discloses that its silicon nitride film extends over the first and second surfaces, Koike does not suggest the desirability of, or provide an objective reason for, forming a silicon nitride layer on both surfaces of other semiconductor substrates. In addition, Koike

teaches away from combination with Tada because the doped areas in Koike are not present while the silicon nitride films encapsulate the substrate. In Koike, the silicon nitride film on the obverse surface side of the substrate is patterned during the formation of the field oxide regions and is removed before the doped areas are formed on the semiconductor substrate. Column 7, lines 11-23; FIGs. 13 and 14. Therefore, the structure in Koike does not have at least one activated, annealed first doped area on its first surface and at least one activated, annealed second, differently doped area within the first doped area while the substrate is encapsulated by the silicon nitride films, as recited in claim 39.

Thus, one of ordinary skill in the art would not be motivated, after reading Koike and Tada, to form an intermediate structure that has a substantially dopant-free, uninterrupted diffusion barrier layer encapsulating the semiconductor substrate, as recited in claim 39.

Since Tada and Koike do not provide one of ordinary skill in the art with any suggestion or motivation to combine the teachings of these references, it is respectfully submitted that a *prima facie* case of obviousness has not been established, as is required to maintain a rejection under 35 U.S.C. § 103(a).

Claims 40, 43, 44, and 45 are allowable, among other reasons, as depending directly from allowable claim 39. A dependent claim is obvious only if the independent claim from which it depends is obvious. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); M.P.E.P. § 2143.03. Claims 40, 43, 44, and 45 depend from claim 39 and, therefore, include all the limitations of claim 39. The nonobviousness of independent claim 39 precludes the rejections of claims 40, 43,

44, and 45 because, as previously discussed, Tada and Koïke do not establish a *prima facie* case of the obviousness of claim 39.

(B) Rejections under 35 U.S.C. § 103(a)-Tada, Koike, and Shim

(1) Arguments for the Patentability of Claims 32 and 49

Claims 32 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tada and Koike and further in view of Shim. Appellants respectfully traverse these rejections as detailed herein.

The teachings of Tada and Koike are as previously summarized.

Shim discloses a method of "forming field oxide isolation regions having sloped edges" that have reduced susceptibility to parasitic bird's beak oxide extension. Column 1, lines 64-67; Column 2, lines 1-4. A silicon nitride or silicon oxynitride layer is applied to one surface of a substrate and is used as a first oxidation resistant layer. Column 3, lines 8-20. The first oxidation resistant layer, in combination with a first pad insulation layer, is patterned to form an active region mask and to expose portions of the substrate that are subsequently oxidized into field oxide isolation regions. Column 3, lines 20-32. A second pad insulation layer is formed on the exposed portions of the substrate and a second oxidation resistant layer is formed over the second pad insulation layer. Column 3, lines 33-54. The second oxidation resistant layer is etched to form oxidation resistant spacers on sidewalls of the active region mask. Column 3, lines 55-58. The second pad insulation layer is grown into field oxide isolation regions having sloped edges. Column 3, lines 58-67. Shim does not disclose that the silicon nitride or silicon

oxynitride layer is applied to both surfaces of the substrate. Shim also does not address the problem of reducing the encroachment of field oxide structures.

(a) Claims 32 and 49

Claims 32 and 49 are dependent claims and depend from independent claims 25 and 46, respectively. A dependent claim is obvious only if the independent claim from which it depends is obvious. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); M.P.E.P. § 2143.03. Claims 32 and 49 depend from independent claims 25 and 46, respectively, and, therefore, include all the limitations of claims 25 and 46. The nonobviousness of these independent claims precludes the rejections of claims 32 and 49 because, as previously discussed, Tada and Koike do not provide a motivation to combine.

Shim is cited by the Examiner for teaching that the oxidation resistant layer comprises silicon oxynitride. Office Action of July 29, 2002, p. 4. However, Shim does not cure the previously identified deficiencies in Tada and Koike with respect to any of the obviousness standards and, as such, does not render claims 25 and 46 obvious.

Specifically, Shim does not provide a motivation to combine to produce the claimed invention because Shim does not suggest the desirability of, or provide an objective reason for, extending the silicon nitride or silicon oxynitride layer over both the first and second surfaces of the semiconductor substrate. Nothing in Shim contemplates encapsulating the semiconductor substrate, let alone encapsulating the semiconductor substrate with the silicon nitride or silicon

oxynitride layer. Shim also does not suggest the desirability of, or provide an objective reason for, using an encapsulated substrate to reduce the encroachment of field oxide structures.

Since Tada, Koike, and Shim do not provide one of ordinary skill in the art with any motivation to combine the teachings of these references, it is respectfully submitted that a *prima facie* case of obviousness of claims 32 and 49 under 35 U.S.C. § 103(a) has not been established.

(E) Appendices

A copy of pending claims 25, 26, 31-34, 37-40, and 43-49, is appended hereto as "Appendix A."

Clean, informal copies of FIGs. 1-8 of the referenced application are appended hereto as "Appendix B."

(F) Conclusion

It is respectfully submitted that a *prima facie* case for the obviousness of claims 25, 26, 31-34, 37-40, and 43-49 of the referenced application has not been established under 35 U.S.C. § 103(a). Therefore, it is respectfully requested that the rejections of claims 25, 26, 31-34, 37-40, and 43-49 as being unpatentable under 35 U.S.C. § 103(a) be withdrawn.

Based on the foregoing reasons, Appellants request:

(A) The reversal of the rejections of claims 25, 26, 31, 33, 34, 37-40, and 43-48 as being unpatentable under 35 U.S.C. § 103(a) over Tada and Koike; and

(B) The reversal of the rejections of claims 32 and 49 as being unpatentable under 35 U.S.C. § 103(a) over Tada and Koike and further in view of Shim.

Respectfully submitted,

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JAW/KAH/ljb
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Attachments: Appendix A and B

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APPENDIX A

25. (Previously seven times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one activated, annealed p-type area within said at least one n-well and at least one activated, annealed n-type area within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

26. (Previously amended) The structure of claim 25 further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

31. (Previously amended) The structure of claim 25, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon nitride.

32. (Previously amended) The structure of claim 25, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.

33. (Previously five times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one activated, annealed doped area within at least one of said at least one n-well and said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

34. The structure of claim 33 further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

37. The structure of claim 33, wherein said substantially dopant-free, uninterrupted diffusion barrier layer comprises one of the group consisting of silicon nitride and silicon oxynitride.

38. (Previously amended) The structure of claim 33, wherein said at least one activated, annealed doped area comprises an impurity selected from the group consisting of an n-type impurity and a p-type impurity.

39. (Previously five times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

at least one activated, annealed first doped area on said substrate first surface;

at least one activated, annealed second, differently doped area within said at least one first doped area; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

40. The structure of claim 39 further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

43. The structure of claim 39, wherein said substantially dopant-free, uninterrupted diffusion barrier layer comprises one of the group consisting of silicon nitride and silicon oxynitride.

44. (Previously amended) The structure of claim 39, wherein said at least one activated, annealed first doped area comprises a p-type impurity and said at least one activated, annealed second, differently doped area comprises an n-type impurity.

45. (Previously amended) The structure of claim 39, wherein said at least one activated, annealed first doped area comprises an n-type impurity and said at least one activated, annealed second, differently doped area comprises a p-type impurity.

46. (Previously three times amended) An intermediate structure useful in the formation of electrical device isolation structures, comprising:

a semiconductor substrate having at least a portion that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;

at least one p-well and at least one n-well defined on said first surface of said substrate;

at least one activated, annealed p-type area defined within said at least one n-well and at least one activated, annealed n-type area defined within said at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

47. (Previously amended) The structure of claim 46 further comprising a layer of oxide between said first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

48. (Previously amended) The structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon nitride.

49. (Previously amended) The structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.

APPENDIX B

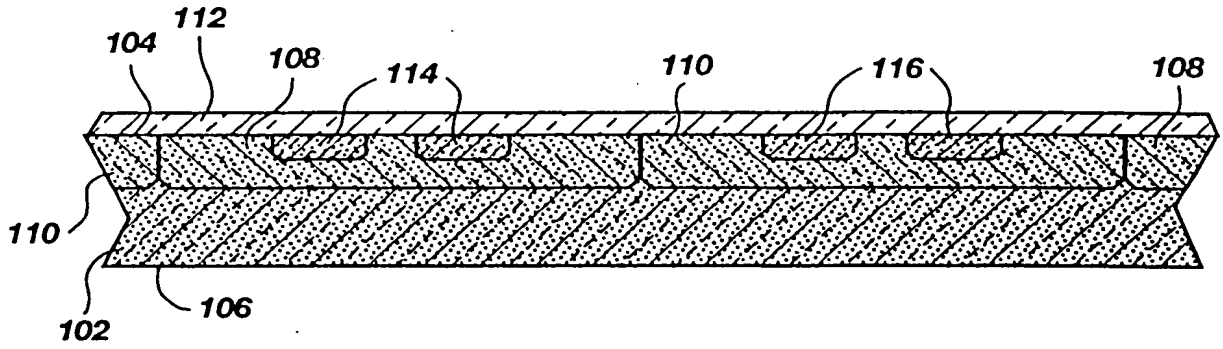

Fig. 1

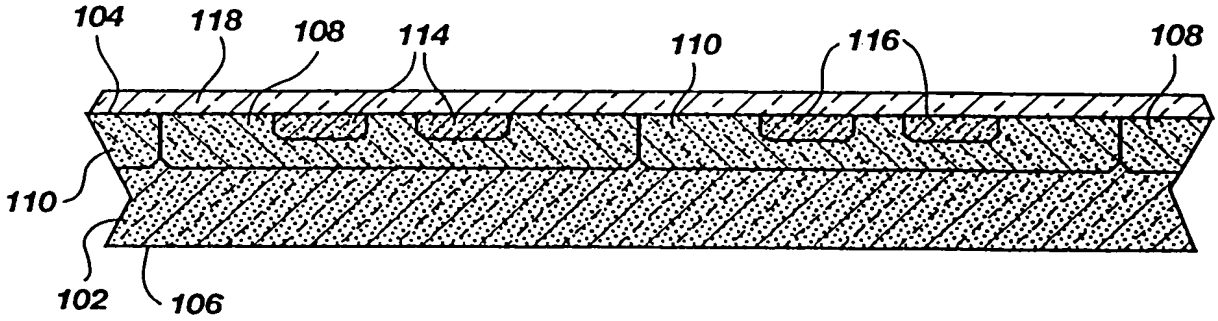

Fig. 2

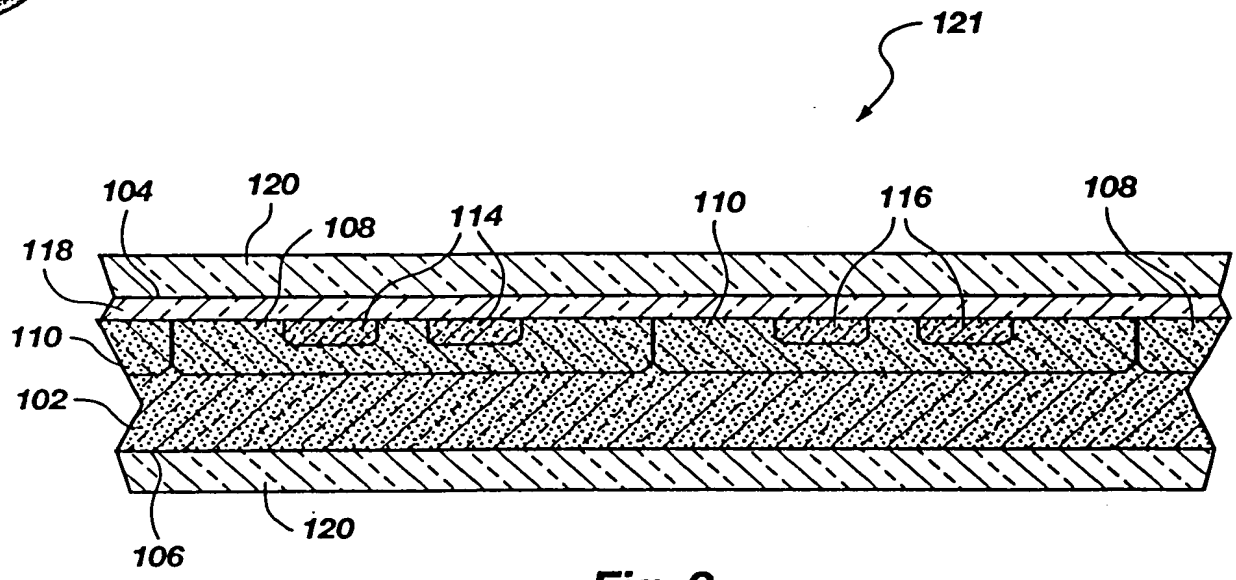

Fig. 3

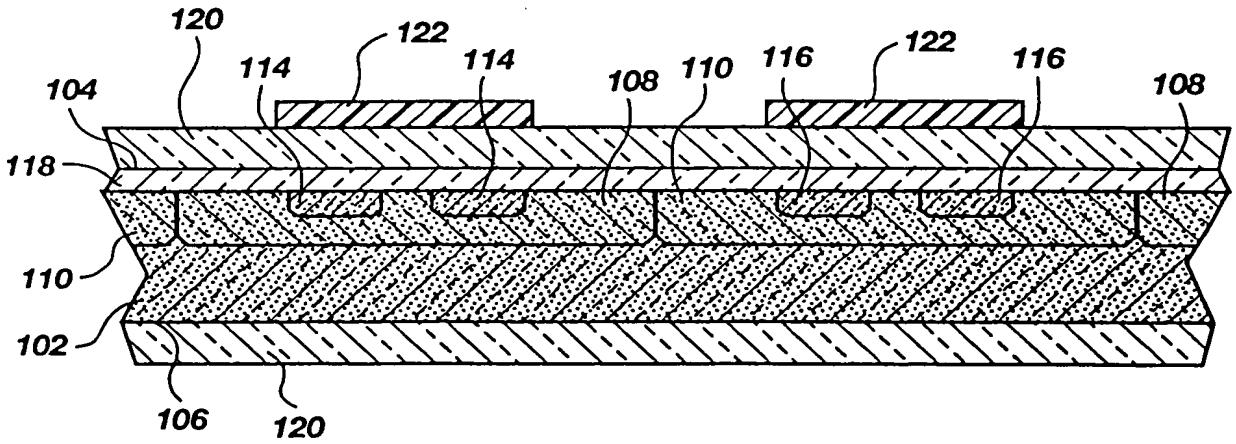

Fig. 4

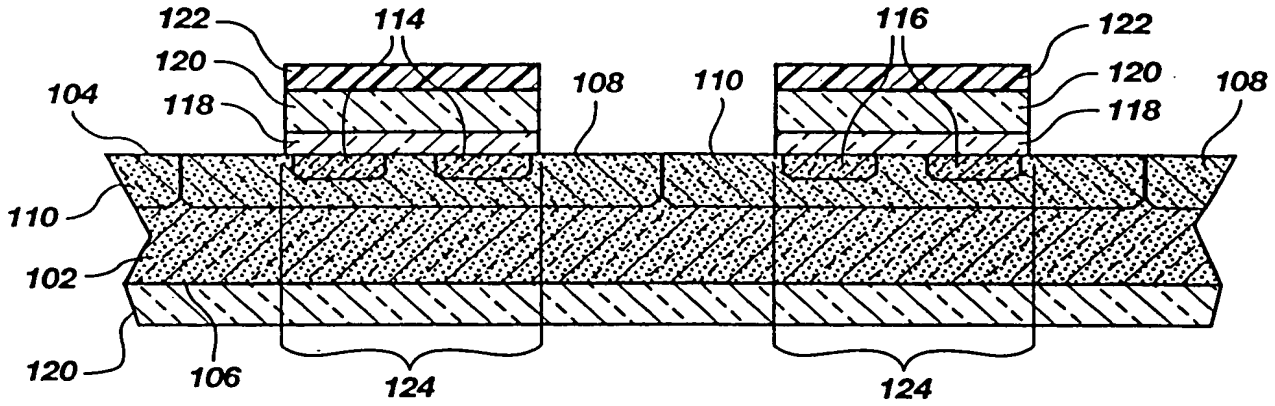

Fig. 5

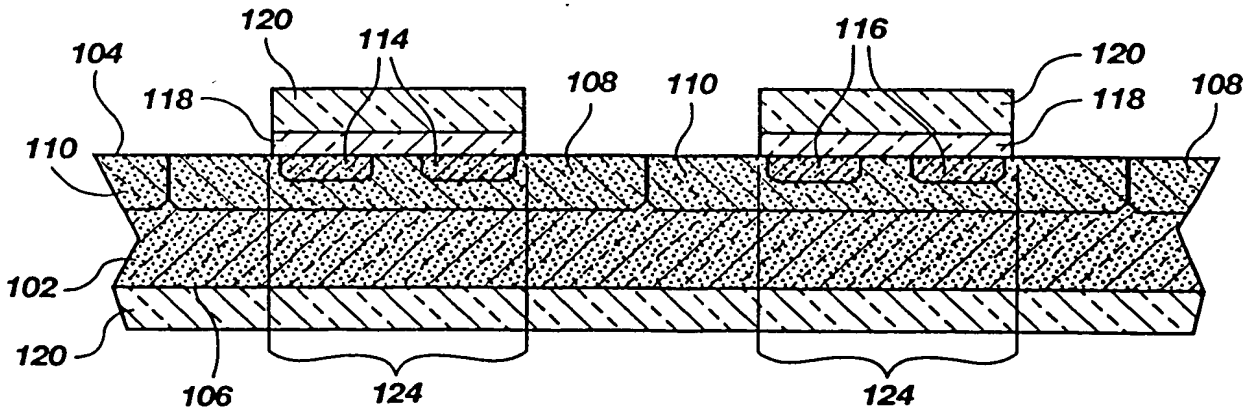

Fig. 6

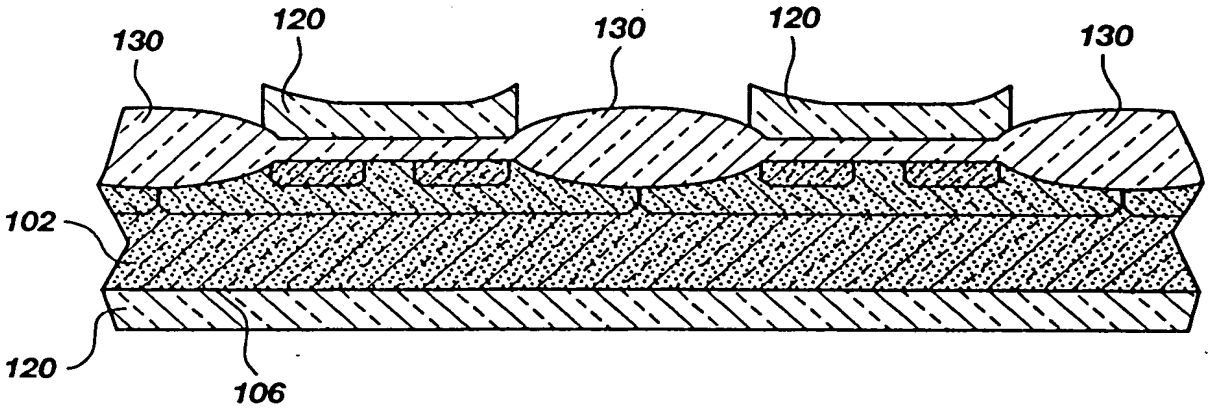

Fig. 7

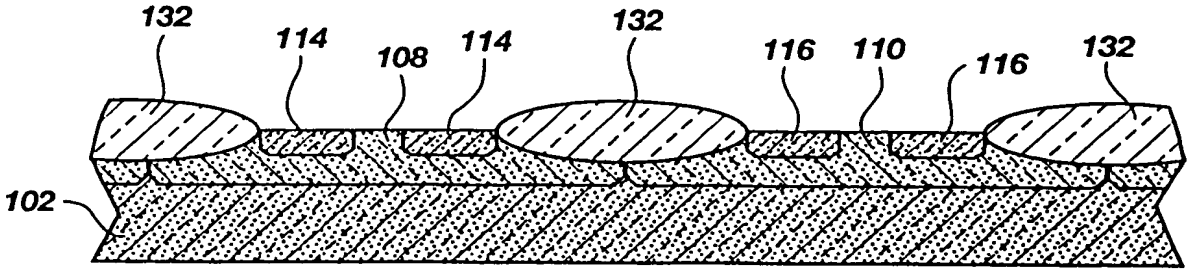

Fig. 8

Ap/f3

PATENT
Attorney Docket No. 2269-3027.2US

2814

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Express Mail Mailing Label Number: EV209825513US

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Person making Deposit: Matthew Wooton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No.: 09/259,145 | Group Art Unit No.: 2814

Filing date: February 26, 1999 | Examiner: Anh D. Mai

For (title): WELL-DRIVE ANNEAL TECHNIQUE USING PREPLACEMENT OF NITRIDE FILMS FOR ENHANCED FIELD ISOLATION

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION — 37 C.F.R. § 192)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on October 21, 2002.

2. STATUS OF APPLICATION
   This application is on behalf of
   - [x] other than a small entity
   - [ ] small entity
     verified statement:
     - [ ] attached
     - [ ] already filed

3. FEE FOR FILING APPEAL BRIEF
   Pursuant to 37 C.F.R. § 1.17(f) the fee for filing the Appeal Brief is:
   - [ ] small entity status $160
   - [x] other than a small entity $320

4. EXTENSION OF TIME
   - [ ] A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.

5. FEE PAYMENT
   - [x] Check No. 3457 is enclosed in payment of the fee for filing the Appeal Brief plus any extension of time for which a petition has been filed.
   - [ ] Please charge this fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

Respectfully submitted,

Joseph A. Walkowski
Reg. No. 28,765
TRASK BRITT, P.C.
P.O. Box 2550
Salt Lake City, UT 84110-2550
(801) 532-1922

Date: December 17, 2002
Enclosures: As identified above